

TITLE OF THE INVENTION
IMAGE PROCESSING APPARATUS AND
PROCESSING METHOD THEREFOR

5 FIELD OF THE INVENTION

The present invention relates to an image processing apparatus for reading an image signal and outputting it and a processing method for the apparatus.

10 BACKGROUND OF THE INVENTION

An image reader, which scans an original in the main scanning direction with a line image sensor (to be referred to as a CCD hereinafter), and at the same time, relatively scans the CCD or the original in the
15 sub-scanning direction (a direction perpendicular to the CCD element arrays), thereby obtaining two-dimensional image information, is known. An example of this type of image reader uses a technique of improving the image read resolution by increasing
20 the number of CCD elements and arranging them in a staggered pattern (refer to Japanese Patent Laid-Open No. 57-141178, Japanese Patent Publication No. 59-6666, and the like).

The arrangement and operation of a standard
25 scanner using a CCD having a staggered pattern will be described with reference to Figs. 14 to 20. Figs. 14A and 14B show a flat bed scanner and, more specifically,

an example of an arrangement for reading a reflected original. Fig. 14A is a plan view of the scanner. Fig. 14B is a side view of the scanner. Reference symbol D denotes an original to be read which is placed
5 on an original glass table 100. A light source 101 irradiates the original D with light. The resultant reflected light is reflected by mirrors 102, 103, and 104 and formed into an image on a CCD 106 through a lens 105. A read unit 107 on which the light source
10 101, mirrors 102, 103, and 104, lens 105, and CCD 106 are fixed is scanned (sub-scanned) parallel to the original glass table 100 from the left to the right in Fig. 14A to read the entire original D, thereby obtaining a 1-page image signal from the CCD 106. A
15 CCD board 113 on which the CCD 106 is mounted is connected to a main board 112 fixed to the image reader through a cable 111. As shown in Fig. 14A, the downward direction is the main scanning direction, and the leftward direction is the sub-scanning direction.
20 This scanner is covered with an outer cover 109 and original press member 110 to shield the original against external light.

Fig. 15 is a block diagram showing control on the operation of the image reader. The electrical signal
25 obtained by photoelectric conversion using the CCD 106 is subjected to gain control in an analog processing circuit 201 including a sample/hold circuit (S/H

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circuit) such as a CDS (Correlated Double Sampling circuit). The resultant signal is then digitized by an A/D converter 202. Reference numeral 204 denotes a shading RAM (Random Access Memory) for storing the light distribution characteristics of the optical system; and 205, an signal processing circuit comprised of a circuit for controlling the shading RAM 204 storing shading correction coefficients and a circuit for controlling enlargement and reduction of image data, i.e., a control circuit for an offset RAM 240 for image read and write. Shading correction is performed by the shading RAM 204. The correction data generated on the basis of shading data obtained by reading a main scanning white reference plate 108 prior to image reading operation is stored in the shading RAM 204. The signal processing circuit 205 using the offset RAM 240, performs not only correction of R, G, and B line offsets but also thinning processing and interpolation processing on the basis of the read image data in magnifying (reducing/enlarging) operation.

Reference numeral 206 denotes a binarizing circuit for binarizing an image signal; and 207, an interface circuit for receiving control signals from an external unit 250 such as a personal computer and outputting image signals.

Reference numeral 208 denotes a CPU (Central Processing Unit) in the form of a microcomputer having

a ROM 208A storing a control program and a RAM 208B serving as a work area. The CPU 208 controls the respective components in accordance with the control program stored in the ROM 208A. Reference numeral 209
5 denotes a timing signal generating circuit for frequency-dividing an output from a quartz oscillator 210 in accordance with the setting in the CPU 208 and generating various types of timing signals.

Fig. 16 shows the arrangement of a color CCD
10 having a staggered element pattern in which two arrays of photodiodes as photoelectric conversion elements are arranged for each color, and the elements are shifted from each other by $1/2$ the element length (to be referred to as $1/2P$ hereinafter) in a staggered pattern.
15 Fig. 17 shows the relationship between photodiodes, shift registers, and first and second transfer clocks ($\phi 1$, $\phi 2$) for one of R, G, and B.

As shown in Figs. 16 and 17, two arrays of photodiodes 5a and 6a are spaced from each other by a
20 distance corresponding to n lines in a sub scanning direction. Image data in the respective element arrays are transferred to shift registers 5c and 6c through shift gates 5b and 6b in accordance with shift pulses SH-r (7). The image data transferred to the shift
25 registers 5c and 6c are sequentially input to an output buffer in accordance with first and second transfer clocks. In this case, the image data from the

photodiodes 5a and 6a are alternately and sequentially transferred to the output buffer, and output from a CCD output OS-r2 in response to each reset clock RS5. The same applies to G and B.

5 The image data transferred to the output buffer are output from CCD outputs OS-g3 and OS-b4 for each reset pulse RS in accordance with the first and second transfer clocks. As a result, as CCD outputs OS-r2, OS-g3, and OS-b4, image data shifted from each other by
10 N lines are output.

Fig. 18 shows an example of the drive timing of the CCD 106 and analog processing circuit 201. Fig. 18 shows the CCD drive timings of $\phi 1(10)$, $\phi 2(11)$, and RS(5), the CCD outputs OS-r2, OS-g3, and OS-b4, an S/H
15 pulse signal in the analog processing circuit for processing the image signals, and the input timing with respect to the A/D converter 202.

The CCD operation defined by the timings of the transfer clocks $\phi 1(10)$ and $\phi 2(11)$ and reset pulse
20 RS(5) will be described with reference to Figs. 19 and 20. Image data is transferred to a floating capacitor in accordance with the transfer clocks $\phi 1(10)$ and $\phi 2(11)$ for driving a transfer electrode and converted into a voltage signal to be output as a signal output
25 OS. At timing Tc1, in Fig. 19, the potential wells of the odd-numbered element array shift register having, image data S_{2n+1} , S_{2n+3} , ... are sequentially

transferred, as shown in Fig. 20. In a state immediately after the reset gate has shifted from the ON state to the OFF state by a reset pulse, no image data is present in the floating capacitor. At timing
5 Tc2, the potential wells in the odd-numbered element array shift register having, the image data S_{2n+1} is transferred to the floating capacitor. At timing Tc3, the reset gate is turned on by a reset pulse, and the image data S_{2n+1} in the floating capacitor is reset.

10 In this manner, image data are alternately transferred from the respective shift registers of the odd- and even-numbered element arrays to the floating capacitor, and the data from the signal output OS is updated by a reset pulse.

15 At a low resolution equal to or less than $1/2$ a basic resolution, data is read from one element array in Fig. 16, as shown in Fig. 21. In this case, the maximum operation frequency of $\phi 1$ and $\phi 2$ is doubled to match the write speed of the RAM with that of the basic
20 resolution, and image data read out after being thinned out by the analog processing circuit 201 (Japanese Patent Laid-Open No. 8-9143). Immediately after a signal is output from each shift register to the output buffer, the output buffer is reset, resulting in a
25 great decrease in CCD output interval. This makes it very difficult to ensure linearity of image data. According to the arrangement of this image reader and

the driving method for the reader, the storage time of the low-resolution mode becomes 1/2 that of the high-resolution mode. If, therefore, the storage time remains unchanged, the read speed of the low-resolution mode must be decreased. That is, it is difficult to make the storage time of the high-resolution mode equal to that of the low-resolution mode and realize high-speed reading operation in the low-resolution mode.

SUMMARY OF THE INVENTION

10 It is an object of the present invention to provide an image processing apparatus and processing method therefor, which can satisfy both the requirements for the balance between the storage time in the high-resolution mode and that in the low-resolution mode and high-speed reading operation in the low-resolution mode.

According to the present invention, the foregoing object is attained by providing an image processing apparatus comprising: image sensing means which includes a first element array having a plurality of photoelectric conversion elements arranged in a line, and a second element array shifted from the first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric conversion elements arranged in a line, and outputs signals of the first and second element arrays from a single output portion; and driving means

having a first mode of reading signals from the second
element array and continuously outputting the signals
from the output portion, and a second mode of reading
signals from the first element array and continuously
5 outputting the signals from the output portion.

According to another aspect of the present
invention, the foregoing object is attained by
providing an image processing apparatus comprising:
image sensing means which includes a first element
10 array having a plurality of photoelectric conversion
elements arranged in a line, and a second element array
shifted from the first element array by a predetermined
distance in a main scanning direction and having a
plurality of photoelectric conversion elements arranged
15 in a line, and outputs signals of the first and second
element arrays from a single output portion; and
driving means for outputting signals from one of the
first and second element arrays and resetting signals
from the other element array in the output portion.

20 In still another aspect of the present invention,
the foregoing object is attained by providing an image
processing apparatus comprising: a first element array
having a plurality of photoelectric conversion elements
arranged in a line; a second element array shifted from
25 the first element array by a predetermined distance in
a main scanning direction and having a plurality of
photoelectric conversion elements arranged in a line; a

first shift register for transferring signals from the first element array; a second shift register for transferring signals from the second element array; and an input unit for receiving at least three pulses

- 5 having different phases and supplying the pulses to the first and second shift registers.

- In still another aspect of the present invention, the foregoing object is attained by providing a processing method for an image processing apparatus
- 10 including a first element array having a plurality of photoelectric conversion elements arranged in a line, a second element array shifted from the first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric
- 15 conversion elements arranged in a line, and output means for outputting signals of the first and second element arrays from a single output portion, comprising the step of reading signals from the second element array and continuously outputting the signals from the
- 20 output portion or reading signals from the first element array and continuously outputting the signals from the output portion.

- In still another aspect of the present invention, the foregoing object is attained by providing a
- 25 processing method for an image processing apparatus including a first element array having a plurality of photoelectric conversion elements arranged in a line, a

second element array shifted from the first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric conversion elements arranged in a line, and output
5 means for outputting signals of the first and second element arrays from a single output portion, comprising the step of outputting signals sent from one of the first and second element arrays from the output portion, and resetting signals from the other element array in
10 the output portion.

In still another aspect of the present invention, the foregoing object is attained by providing a processing method for an image processing apparatus including a first element array having a plurality of
15 photoelectric conversion elements arranged in a line, and a second element array shifted from the first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric conversion elements arranged in a line,
20 comprising the step of transferring signals from the first and second element arrays in accordance with at least three pulses.

Other features and advantages of the present invention will be apparent from the following
25 description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a timing chart showing CCD driving operation for reading out data from only an
5 odd-numbered element array of the first embodiment;

Fig. 2 is a timing chart showing CCD driving operation for reading data from only an even-numbered element array of the first embodiment;

Fig. 3 is a timing chart showing CCD driving
10 operation in a basic resolution mode to explain the first embodiment;

Fig. 4 is a timing chart showing CCD driving operation in a basic resolution mode of the prior art compared with the first embodiment;

Fig. 5 is a timing chart showing CCD driving
15 operation in a low-resolution mode to explain the first embodiment;

Fig. 6 is a view showing read image areas in the basic resolution mode to explain the first embodiment;

Fig. 7 is a block diagram showing the internal
20 structure of a CCD to explain the second embodiment of the present invention;

Fig. 8 is a schematic diagram of photodiode portions and shift register portions in the CCD in
25 Fig. 7;

Fig. 9 is a timing chart for explaining CCD driving operation using the arrangement in Fig. 7;

Fig. 10 is a view for explaining operation in the CCD at the CCD driving timing in Fig. 9;

Fig. 11 is a timing chart for explaining CCD driving operation using the arrangement in Fig. 7;

5 Fig. 12 is a timing chart for explaining another CCD driving operation using the arrangement in Fig. 7;

Fig. 13 is a timing chart for explaining still another CCD driving operation using the arrangement in Fig. 7;

10 Figs. 14A and 14B are schematic views of an image reader;

Fig. 15 is a block diagram of a circuit for controlling the image reader;

15 Fig. 16 is a block diagram showing the internal structure of a CCD to explain the prior art;

Fig. 17 is a wiring diagram of photodiode portions and shift register portions in the CCD in Fig. 16;

20 Fig. 18 is a view for explaining an example of a conventional CCD element array;

Fig. 19 is a timing chart showing CCD driving operation to explain the prior art;

25 Fig. 20 is a view for explaining operation in the CCD at a CCD driving timing according to the prior art; and

Fig. 21 is a timing chart showing CCD driving operation with a resolution $1/2$ the basic resolution to

explain the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be
5 described below with reference to the accompanying
drawings.

(First Embodiment)

A scanner according to the first embodiment of
the present invention will be described with reference
10 to Figs. 1 to 4.

Since the mechanical and electrical arrangements
of the scanner according to this embodiment are the
same as those shown in Figs. 14 to 17, a description
thereof will be omitted.

15 Figs. 1 and 2 are timing charts showing transfer
clocks $\phi 1$ and $\phi 2$ and reset clock RS according to this
embodiment, and an output signal OS-r (OS-g and OS-b)
as the result obtained by driving shift registers using
these clocks.

20 Fig. 1 will be described first. Referring to
Fig. 1, like Fig. 18, the transfer clocks $\phi 1$ and $\phi 2$
have opposite phases. At the leading edge of the clock
 $\phi 1$, image data in the odd-numbered elements (image
data stored in the lower shift register in Fig. 17) is
25 outputted to the output buffer. At the trailing edge
of the clock $\phi 1$, image data in the even-numbered
elements (image data in the upper shift register in

Fig. 17) is outputted to the output buffer.

The reset clock RS goes HIGH at the instant when $\phi 1 = \text{LOW}$ and $\phi 2 = \text{HIGH}$. With this operation, the image data in the even-numbered elements is reset at the same time it is outputted to the output buffer, and hence is not output from the CCD. As a consequence, as indicated by the lowermost level in Fig. 1, only the image data from the odd-numbered elements are output from the CCD.

In contrast to this, in the case shown in Fig. 2, the reset clock RS goes HIGH at the instant when $\phi 1 = \text{HIGH}$ and $\phi 2 = \text{LOW}$. With this operation, the image data from the odd-numbered elements are reset at the same time it is outputted from the shift register to the output buffer, and hence is not outputted from the CCD. As a consequence, as indicated by the lowermost level in Fig. 2, only the image data from the even-numbered elements is outputted from the CCD.

As shown in Figs. 1 and 2, the CCD can selectively output only the image data read by either the odd or even photodiode arrays. And then, even if the frequencies of the transfer clocks $\phi 1$ and $\phi 2$ and reset clock RS are increased twice those in the prior art, sufficient output time can be ensured for image data in each element which is outputted from the output buffer. More specifically, as compared with the case shown in Fig. 21 in which image in all the elements are

outputted from the CCD and thinned out by the S/H circuit, with the operation shown in Figs. 1 and 2, the interval between the instant at which image data is outputted from the shift register to the output buffer and the instant at which the image data is reset is long, and hence the precision of outputting data from the CCD (output buffer) improves.

Fig. 3 is a timing chart showing a case where an image is read in a high-resolution mode by driving the respective clocks at the timings shown in Figs. 1 and 2. In this embodiment, as shown in Fig. 3, first, the respective clocks are driven as shown in Fig. 1 to continuously output only the image data in the odd-numbered element array of the CCD to the memory. The respective clocks are then driven as shown in Fig. 2 to continuously output the image data in the even-numbered element array to the memory. Fig. 4 is a timing chart showing how data is read by driving the respective clocks in the prior art. "T" in Fig. 4 indicates the time required to output image data from the CCD to the memory from all the elements arranged in a staggered pattern. Referring to Fig. 3, the frequencies of the respective clocks are increased to twice those in the prior art to output from the CCD, the image data in the odd-numbered elements, in the time interval of $T/2$, and output the image data from the CCD in the even-numbered elements in the next time

interval of $T/2$. In the high-resolution mode, therefore, the data in all the photoelectric conversion elements of the two arrays can be outputted in the same period of time as that in the prior art. Even if a
5 limitation is imposed on the DRAM access time on the digital circuit, and the same CCD output timing as that of the prior art is required, data can be read in a storage time $1/2$ of that of the prior art.

Fig. 5 is a timing chart showing how an image is
10 read in a low-resolution mode of this embodiment. In this embodiment, in the low-resolution mode, the respective clocks are always driven as shown in Fig. 1 to output only the image data in the odd-numbered elements from the CCD. Obviously, the present
15 invention is not limited to this, and the respective clocks may always be driven as shown in Fig. 2 to output from the CCD only the image data in the even-numbered elements. In addition, in the low-resolution mode, since the CCD moves in the
20 sub-scanning direction at a speed twice that of the high-resolution mode, data can be read at high speed.

Furthermore, since the frequencies of the respective clocks remain the same in the high-resolution mode and low-resolution mode, the
25 storage time also remains the same.

If a distance between the odd and even photodiode arrays comprising $a \times a$ photodiodes is set to an odd

multiple of $a/2$, and the CCD is driven in the same manner as in this embodiment, read areas like those shown in Fig. 6 can be obtained.

According to the arrangement of the image reader
5 using the CCD having a staggered pattern according to this embodiment and the driving method for the image reader, data can be read from either the odd-numbered element array or even-numbered element array in the staggered pattern, and element addition is allowed in
10 the shift register unit to read data from the CCD in $1/2$ the storage time of the prior art in the basic resolution (high-resolution) mode. In the mode of reading data with a resolution $1/2$ that of the basic resolution mode, data can be read in the same storage
15 time as that of the basic resolution mode. Therefore, the same original can be read in a time $1/2$ the read time of the basic resolution mode.

Therefore, both the requirements for the balance between the storage time in the high-resolution mode
20 and that in the low-resolution mode and high-speed reading operation in the low-resolution mode can be satisfied.

(Second Embodiment)

A scanner according to the second embodiment of
25 the present invention will be described next with reference to Figs. 7 to 13. The mechanical arrangement of the scanner according to this embodiment is the same

as that shown in Figs. 14 and 15, and hence a description thereof will be omitted.

Fig. 7 is a view showing the CCD arrangement according to the second embodiment in the image processing apparatus according to the present invention.

Like Fig. 16, Fig. 7 shows the arrangement of the color CCD having a staggered arrangement in which two arrays of photodiodes are arranged for each color, and the respective elements are shifted from each other by 1/2 the element length in a staggered pattern. This scanner has a first transfer clock 10 ($\phi 1$), second transfer clock 11 ($\phi 2$), and third transfer clock 12 ($\phi 3$). Fig. 8 is a view showing the relationship between the photodiodes, shift registers, first transfer clock ($\phi 1$), second transfer clock ($\phi 2$), and third transfer clock ($\phi 3$) for one color of R, G, and B. The number of shift registers is twice or more that of photodiodes.

Referring to Fig. 7, in the photosensitive portion for R, photodiode arrays 5a and 6a are arranged at a distance n from each other. Image data in the respective element arrays are transferred to shift registers 5c and 6c through shift gates 5b and 6b in accordance with shift pulses SH-r (7). The image data transferred to the shift registers 5c and 6c are sequentially transferred in response to the first, second, and third transfer clocks $\phi 1$, $\phi 2$, and $\phi 3$.

The image data is alternately and sequentially inputted from the photodiode arrays 5a and 6a to the output buffer. The arrangements and operations of the photosensitive portions for G and B are the same as those described above for R. Since these photosensitive portions are spaced apart from each other by N lines as shown in Fig. 7, image data shifted from each other by N lines are output as CCD outputs OS-r (2), OS-g (3), and OS-b (4).

A method of reading image information with a resolution 1/4 or less than the basic resolution of the scanner using the CCD shown in Figs. 7 and 8 will be described with reference to Figs. 9 and 10.

Fig. 9 is a timing chart for explaining the timings of the transfer clocks $\phi 1$, $\phi 2$, and $\phi 3$ and a reset pulse RS in this embodiment. In the embodiment, the frequency of the transfer clock $\phi 1$ is set to be twice that of each of the transfer clocks $\phi 2$ and $\phi 3$, and the image data in the odd-numbered element array is reset by the reset pulse RS to be discarded.

Fig. 10 is a view showing the states of potential wells and data transfer at each timing in Fig. 9. In the shift register for the even-numbered element array, at timing Tbl in Fig. 9, image data S_{2n} , S_{2n+2} ,...

before element addition in the shift register portion, are secured in the potential wells, as indicated by the uppermost level in Fig. 10. Since the reset gate has

been turned on by a reset pulse immediately before this state, no image data exists in the floating capacitor.

At a timing Tb2, the transfer clock $\phi 1$ goes HIGH to transfer image data S2n+2, S2n+6, and S2n+10 without
5 transferring image data S2n, S2n+4, and S2n+8. At a timing Tb3, the reset gate is turned on by a reset pulse to reset the image data in the floating capacitor. At the same time, only the image data S2n+2, S2n+6, and S2n+10 transferred at the timing Tb2 are further
10 transferred to be added to the image data S2n, S2n+4, and S2n+8, respectively.

At timings Tb4 and Tb5, the added image data are shifted on the shift register. At these timings, as shown in Fig. 10, the image data S2n+S2n+2 is shifted
15 to the floating capacitor to electrically connect a power supply OD to a signal output OS, thereby outputting a signal OS.

At a timing Tb6, the reset gate is turned on by a reset pulse to reset the image data in the floating
20 capacitor, and the added image data is shifted on the shift register. At timings Tb7 and Tb8, the added image data are shifted on the shift register. As a consequence, the same state as that at the timing Tb2 is set. Subsequently, as the timings are sequentially set, Tb3 \rightarrow Tb4 \rightarrow ..., the added image data is
25 sequentially output from the CCD as outputs OS. Thus, data can be output from the CCD as shown in Fig. 11.

Fig. 12 shows a preferable embodiment of the 1/4-resolution read mode. In this preferable embodiment clocks $\phi 1$, $\phi 2$, $\phi 3$, and RS is driven to change potential state in a cycle of Tb2 \rightarrow Tb3 \rightarrow Tb5 \rightarrow Tb6 \rightarrow Tb2 \rightarrow Tb3 $\rightarrow \dots$, in Fig. 9, with an omission of an illustration concerning the timings Tb1, Tb4, Tb7, and Tb8, so that data can be efficiently shifted and the precision in outputting data from the output buffer can be improved when compared with Fig. 9.

According to the operation of this embodiment, the signals obtained by adding data in adjacent elements in the even-numbered element array is sequentially output as the CCD outputs OS-r, OS-g, and OS-b. By adding adjacent image data, data having a resolution 1/4 that of the high-resolution mode is outputted to the RAM for each line, as shown in Fig. 13. This makes it possible to increase the frequencies of the transfer clocks and reset clock by four times and decrease the storage time for each line to 1/4 without changing the transfer rate with respect to the RAM. Therefore, image reading operation can be performed with 1/4 the resolution at quadruple speed. Even if, a limitation is imposed on the DRAM access time on the digital circuit, and the same CCD output timings as those shown in Figs. 3 to 5 are required, one line can be read in a time 1/4 that of the high-resolution mode.

According to this embodiment, in the color CCD having the staggered arrangement in which the respective elements are shifted from each other by $1/2P$ in a staggered pattern, shift registers twice or more
5 in number than photodiodes are arranged, and the transfer clock $\phi 3$ is prepared in addition to the transfer clocks $\phi 1$ and $\phi 2$. In addition, this CCD includes the driving control means for controlling the potential level of the shift register portion with the
10 respective transfer clocks, the reset means which uses a reset pulse to read out image data from either the odd- or even-numbered element array in the low-resolution mode, and the transfer means for performing CCD transfer which allows addition of data
15 in adjacent elements in the shift register portion.

In this case, image data is reset by the reset clock RS to read image data from either the odd- or even-numbered element array. In the low-resolution mode, the time required to read one line is shortened
20 by adding data in elements in the shift register portion in the low-resolution mode without decreasing the S/N ratio.

As described above, in the read mode with a resolution $1/4$ the basic resolution, the same original
25 can be read in a time $1/4$ that in the basic resolution mode with a storage time $1/2$ that in the basic-resolution mode without decreasing the S/N ratio.

With the arrangement shown in Figs. 7 and 8, the first embodiment can be implemented by inputting the same signals as the signals $\phi 2$ and $\phi 3$.

That is, the operation in the high-resolution
5 mode and low-resolution mode in the first embodiment shown in Figs. 3 and 5 can be implemented by using the arrangement of the second embodiment.

As has been described above, according to the above embodiment, the first and second element arrays
10 are shifted from each other by a predetermined width, and data can be read from either the first or second element array. Therefore, data can be read out from either the odd- or even-numbered element array. This makes it possible to satisfy both the requirement for
15 the balance between the storage times in the high-resolution mode and low-resolution mode and the requirement for high-speed reading operation in the low-resolution mode.

As many apparently widely different embodiments
20 of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.